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POWER AND DELAY OPTIMIZATION IN FULL ADDER CIRCUIT USING DIFFERENT TECHNIQUES

R. SUGANYA & K. S. NATIYAA

VLSI Design Department & Anna University Tagore Institute of Engineering and Technology, Deviyakurichi, India

ABSTRACT

The Full Adder circuit is an important component in application such as Digital Signal Processing (DSP) architecture, microprocessor, microcontroller and data processing units. This paper discusses the evolution of full adder circuits in terms of lesser power consumption and higher speed. Starting with the most conventional 28 transistors full adder and then gradually studied different types of full adders. This paper has also included some of the most popular full adder cells like Transmission gate full adder, pass transistor full adder, Static Energy Recovery Full Adder (SERF), Adder9B, GDI based full adder and Self resetting logic(SRL) with GDI full adder. The simulations have been carried out by Tanner EDA tools on 250nm technology.

KEYWORDS: CMOS Transmission Gate (TG), Pass-Transistor Logic (PTL), Complementary Pass-transistor Logic (CPL), Gate Diffusion Input (GDI), Static Energy Recovery Full Adder (SERF)), Adder 9B, GDI based Full Adder, low power, Full Adder, CMOS, exclusive-OR (XOR), exclusive-NOR (XNOR), Self Resetting Logic(SRL)